UNITED STATES PATENT APPLICATION FOR

METHODS, ALGORITHMS, SOFTWARE, ARCHITECTURES, SYSTEMS AND
CIRCUITRY FOR ADAPTIVE FILTERING AND/OR MINIMIZING A SEQUENCE
DETECTOR ERROR RATE

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RELATED APPLICATIONS

[0001]   This application claims the benefit of U.S. Provisional Application No. 60/457,661, filed March 25, 2003 (Attorney Docket No. MP0307PR).

FIELD OF THE INVENTION

5   [0002]   The present invention generally relates to the field of adaptive algorithms, software and filters, and methods for minimizing a sequence detector error rate.   More specifically, embodiments of the present invention pertain to methods, algorithms, software, architectures, systems and circuits for targeting certain dominant error types in an adaptive FIR filter and/or signal equalizer.

10   DISCUSSION OF THE BACKGROUND

[0003]   Finite impulse response (FIR) channel filters are the most commonly used type of digital equalizer for commercially produced digital receivers. FIG. 1 shows a block diagram of a system 10 employing such a filter. A digital data signal X is received in FIR filter or equalizer 12, which filters the signal X according to a filtering algorithm (discussed in more detail below)

15   to produce an equalized data signal Y. The equalized data signal Y is processed sequentially by a sequence detector 14 and a target filter 16 to produce an ideal, noiseless value YH for the equalized data signal. The difference between equalized data signal Y and its ideal, noiseless value YH is the error by which the filtering algorithm is adapted (see the discussion below).

[0004]   Such filters have a transfer function that generally satisfies the following

20   equations:

$$\text{FIR filter} = (C0, C1, \ldots Cn) \qquad\qquad (1)$$

$$Y[k] = C0*X[k] + C1*X[k-1] + C2*X[k-2] + \ldots + Cn*X[k-n] \qquad (2)$$

where C is a weighting coefficient and Y[k] is the output of the filter.

[0005]   Adaptive FIR filter algorithms generally allow for self-optimization of channel parameters. Regular least mean squares (LMS) gradient algorithms, which are the most common technique for adaptive FIR filtering, generally include a set of update rules for the coefficients of equations (1) and (2) above as follows:

$$C0 = C0 + \mu*E[k]*X[k] \qquad (3)$$

$$C1 = C1 + \mu*E[k]*X[k-1] \qquad (4)$$

$$\ldots$$

$$Cn = Cn + \mu*E[k]*X[k-n] \qquad (5)$$

where μ is a weighting coefficient or factor that affects or controls the adaptation rate of the filter, and E[k] is the error in the Y[k] value relative to its ideal noiseless value (e.g., YH in the flow shown in FIG. 1).

[0006]   The ideal noiseless value YH is usually estimated and/or generated by convolving the output of the sequence detector with the target channel response (see step 28 in the flow chart 20 shown in FIG. 2). Thus, the next value of the coefficients Cx in equations (1) and (2) above depends on their previous value. The occasional errors in the estimated noiseless values due to detection errors do not materially impact the convergence of the regular LMS algorithm.

[0007]   FIG. 2 shows a flow chart for a conventional adaptive filtering process 20 employing the system 10 of FIG. 1. The process begins with step 22, receiving a data signal X

into a conventional data receiver circuit, system and/or apparatus. Step 24 generally involves passing the data X through an FIR filter (e.g., FIR filter 12 of FIG. 1) to generate equalized data signal Y. The primary function of FIR filter 12 is to output equalized data Y to a downstream receiving and/or processing device.

5   [0008]   However, one may also train, update, correct and/or modify the filtering algorithm to ensure a desired or predetermined level of accuracy in the equalizing process. The first step of the conventional training sub-process is step 26, processing the equalized data signal in a sequence detector. Thereafter, in step 28, the sequence-detected equalized data signal is convolved with a target filter to estimate or generate YH. The target filter generally results from

10   user selection of the channel target, which is generally an ideal sequence detector filter, in step 30. The difference between equalized data signal Y and ideal, noiseless equalized data signal YH is then calculated in step 34, and in step 36, that error information (i.e., a non-zero difference between Y and YH) is fed into the FIR filter to update and/or modify the weighting coefficients in the FIR algorithm.

15   [0009]   The regular LMS algorithm reduces the root-mean-square (RMS) error of the E[k] values and generally results in a fairly low error rate after a period of time in which the coefficients converge. However, the lowest RMS error for Y[k] still does not equate to the lowest error rate for Viterbi detection. For example, in data receivers used in magnetic recording applications (e.g., read channel devices), errors are often dominated by simple error events such

20   as single bit, dibit or tribit errors. Minimizing the RMS error in Y[k] indirectly minimizes these error events in some fashion, but not necessarily optimally. Conventional receivers and filtering algorithms tend to sacrifice performance in order to optimize detection of all types of error patterns. A need is thus felt for an approach that directly targets minimizing one or more dominant or relatively frequent error events to improve or maintain detection performance and/or

25   reduce convergence time.

SUMMARY OF THE INVENTION

[0010]   Embodiments of the present invention relate to methods, algorithms, software, systems, architectures and circuitry for adaptively filtering a data stream that minimizes dominant error events. The method and algorithm, which are generally directed to modifying or updating

5   an adaptive algorithm for processing data, generally comprise the steps of (a) processing a data sequence in accordance with the adaptive algorithm to produce a processed data sequence; (b) filtering the data sequence with a first set of filter characteristics to generate a filtered data term for the adaptive algorithm; (c) generating a filtered error term for the adaptive algorithm from at least the processed data sequence using a second set of filter characteristics, the second set of

10   filter characteristics being similar to the first set of filter characteristics; and (d) updating the adaptive algorithm in response to the filtered data term and the filtered error term. The software is generally configured to implement one or more aspects of the inventive methods disclosed herein.

[0011]   The present signal processing architecture generally comprises (i) an equalizer

15   configured to equalize and/or filter a data sequence in accordance with an adaptive algorithm and provide an equalized data output; (ii) a first filter, configured to receive the data sequence and generate a filtered data term for the adaptive algorithm; and (iii) an error term circuit, configured to receive the equalized data output and provide a filtered error term for the adaptive algorithm, the error term circuit comprising a second filter having filter characteristics similar to the first

20   filter. The present systems generally include the architecture and, for example, a receiver and/or magnetic recording device.

[0012]   The present invention advantageously provides improved convergence speed relative to conventional LMS algorithms for FIR filtering of digital data, and approaching best-in-class adaptive LMS algorithms. At the same time, the present invention advantageously

25   provides improved performance relative to LMS algorithms that are best-in-class for

convergence speed. In certain embodiments, performance provided by the present invention may approach best-in-class LMS algorithms performance in reducing overall RMS error.

[0013]   These and other advantages of the present invention will become readily apparent from the detailed description of preferred embodiments below.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0014]   FIG. 1 is a diagram showing a conventional regular LMS gradient FIR filtering system/architecture.

[0015]   FIG. 2 is a flow chart for the conventional regular LMS gradient FIR filtering
5   process of FIG. 1.

[0016]   FIG. 3 is a flow chart for an embodiment of the present adaptive FIR filtering process.

[0017]   FIGS. 4A and 4B show examples of single bit error detection in accordance with the present invention.

10   **[0018]**   FIG. 5 shows examples of dibit error detection in accordance with the present invention.

[0019]   FIG. 6 is a block diagram showing a first embodiment of an architecture configured to implement the adaptive FIR filtering process of FIG. 3.

[0020]   FIG. 7 is a block diagram of a hardware embodiment for updating the adaptive
15   FIR filter of FIG. 6.

[0021]   FIG. 8 is a block diagram showing a second embodiment of an architecture configured to implement the adaptive FIR filtering process of FIG. 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022]   Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they

5   are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be readily

10   apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present invention.

[0023]   Some portions of the detailed descriptions which follow are presented in terms of

15   processes, procedures, logic blocks, functional blocks, processing, and other symbolic representations of operations on data bits, data streams or waveforms within a computer, processor, controller and/or memory. These descriptions and representations are generally used by those skilled in the data processing arts to effectively convey the substance of their work to others skilled in the art. A process, procedure, logic block, function, process, etc., is herein, and

20   is generally, considered to be a self-consistent sequence of steps or instructions leading to a desired and/or expected result. The steps generally include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical, magnetic, optical, or quantum signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer or data processing system. It has proven convenient at

25   times, principally for reasons of common usage, to refer to these signals as bits, waves, waveforms, streams, values, elements, symbols, characters, terms, numbers, or the like.

[0024]   It should be borne in mind, however, that all of these and similar terms are associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise and/or as is apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms

5   such as "processing," "operating," "computing," "calculating," "determining," "manipulating," "transforming," "displaying" or the like, refer to the action and processes of a computer or data processing system, or similar processing device (e.g., an electrical, optical, or quantum computing or processing device), that manipulates and transforms data represented as physical (e.g., electronic or magnetic) quantities. The terms refer to actions and processes of the

10   processing devices that manipulate or transform physical quantities within the component(s) of a system or architecture (e.g., registers, memories, other such information storage, transmission or display devices, etc.) into other data similarly represented as physical quantities within other components of the same or a different system or architecture. Thus, the terms "process" and "function" (and grammatical variations thereof) may also refer to and encompass any circuit or

15   block of circuitry that performs the process or function.

[0025]   Furthermore, for the sake of convenience and simplicity, the terms "data," "data stream," "signal," "waveform," "sequence" and "information" may be used interchangeably, as may the terms "connected to," "coupled with," "coupled to" and "in communication with;" the terms "filter" and "convolve" (and grammatical variants thereof); and the terms "modify,"

20   "alter," "adapt" and "update" (and grammatical variants thereof), but these terms are generally given their art-recognized meanings.

[0026]   The present invention concerns a method, algorithm, system, architecture and circuitry for adaptively filtering a digital data stream. The method generally comprises the steps of (a) processing a data sequence in accordance with the adaptive algorithm to produce a

25   processed data sequence; (b) filtering the data sequence with a first set of filter characteristics to generate a filtered data term for the adaptive algorithm; (c) generating a filtered error term for the

adaptive algorithm from at least the processed data sequence using a second set of filter characteristics, the second set of filter characteristics being similar to the first set of filter characteristics; and (d) updating the adaptive algorithm in response to the filtered data term and the filtered error term. A further aspect of the invention concerns software configured to

5   implement and/or encode one or more of the methods disclosed herein.

[0027]   A still further aspect of the invention concerns a signal processing architecture comprising (i) an equalizer configured to equalize and/or filter a data sequence in accordance with an adaptive algorithm and provide an equalized data output; (ii) a first filter, configured to receive the data sequence and generate a filtered data term for the adaptive algorithm; and (iii) an

10   error term circuit, configured to receive the equalized data output and provide a filtered error term for the adaptive algorithm, the error term circuit comprising a second filter having filter characteristics similar to the first filter. An even further aspect of the invention concerns a system including the architecture and, for example, a receiver or a magnetic recording device.

[0028]   The invention, in its various aspects, will be explained in greater detail below with

15   regard to exemplary embodiments.

An Exemplary Method and Algorithm

[0029]   In one aspect, the present invention relates to a method and algorithm for modifying an adaptive algorithm for processing data, comprising the steps of (a) processing a data sequence in accordance with the adaptive algorithm to produce a processed data sequence;

20   (b) filtering the data sequence to generate a filtered data term for the adaptive algorithm; (c) filtering an error term for the adaptive algorithm generated from at least the processed data sequence, each of the filtering steps using a similar or identical set of filter characteristics; and (d) updating the adaptive algorithm in response to the filtered data term and the filtered error term. As will be explained below, the data sequence generally comprises digital data, and may

comprise, for example, a digital data stream received in a data signal receiver, an equalized or filtered digital data stream, a processed digital data sequence, and/or an equalized sequence-processed digital data signal. The method and algorithm target certain error events that tend to dominate the set of errors in a given application, thereby improving the convergence rate without

5   sacrificing performance (or filtering quality). In a preferred embodiment, a dominant error type comprises greater than 50% of the error events for the data processing application. In certain embodiments, the dominant error type comprises 80% or more of the error events.

[0030]   For example, magnetic recording applications generally use read channel devices to receive and process magnetically recorded data. In read channel devices, when the recording

10   density is below a certain threshold, single-bit error events can dominate the entire set of error events that occur in reading and processing magnetically recorded data. Exemplary recording density thresholds may be linear and/or areal, and may be 500 Mbit/in^2 or higher, preferably 5 Gbit/in^2 or higher, and more preferably 50 Gbit/in^2 or higher. Alternatively and/or additionally, exemplary recording density thresholds may be measured in flux changes per inch (FCI), and

15   may be 50 kFCI or higher, preferably 100 kFCI or higher, and more preferably 500 kFCI or higher. In this case, targeting single-bit errors for minimization in the adaptive filtering algorithm may generate a lower sequence detection error rate.

[0031]   FIG. 3 shows a flow chart for an exemplary process and/or algorithm 100 that targets certain dominant types of errors for minimization in adaptive filtering. As with FIG. 1, in

20   first step 102, a digital data stream is received, for example in a conventional digital signal receiver. The primary function of the process 100 is reflected in step 104, in which the received digital data stream is equalized by processing it through a FIR filter to generate a data out signal D_{OUT}, similarly to FIGS. 1-2. The invention focuses on how the FIR filter is updated, using a new algorithm that targets certain predominant and/or fundamental error types.

[0032]   For example, in an analysis for single-bit error events, one convolves the equalized data signal Y[k] through a matched filter and an error event filter (see, e.g., step 106 in FIG. 3).   While a matched filter and error filter are particularly suited for the exemplary embodiment described herein, any filter suited for a particular application may be used. In this

5   exemplary application, the error event filter may be optimized for minimizing RMS single-bit errors. The general equation for this part of the process is:

$$MFY[k] = Y[k] * \text{Matched-Filter} * \text{Error-Filter} \qquad (6)$$

[0033]   The "matched filter" is a function that generally reverses the order of a given data sequence with respect to time. For example, if the channel from which the data sequence is taken has a target response of (a0, a1, a2, ... an), the matched filter for this channel is just the

10   transposition, or reverse sequence, of the channel response: (an, ... a2, a1, a0). In the invention, n can be any integer such that the channel response and/or data sequence is capable of being processed by existing and/or the inventive circuitry and software. In preferred embodiments, n is at least 2, preferably at least 3. In common implementations of adaptive FIR filters for data

15   signal processing, n is from 7 to 11 (i.e., the response or filter length is from 8 to 12 bits long).

[0034]   In this embodiment, the error filter is an exact filter; that is, the error filter corresponds to the error itself. For example, the error filter for a single bit error is just the unit function (1).   However, the invention is not limited to optimizing for single bit errors; for example, the optimized error filter for dibit error events is the (1,-1) function, the optimized error

20   filter for tribit error events is (1,-1,1), etc. Depending on the application, this error filter list can be extended (e.g., to include four-bit, five-bit and/or larger error events), resized (e.g., to target minimization of error events of at least x bits, where x is an integer of 2, 3, 4 or more) and/or truncated (from x bits to y bits, where x is as described *infra* and y is an integer $\geq$ x+1, x+2, etc.) as needed or desired. Of course, these error functions also include their complements, which are

25   mathematically equivalent to the recited error filter functions.

[0035]   Minimizing the output of the matched-filtered equalized data sequence MFY[k] should minimize the error rate for that particular error event. However, issues that now arise include how to minimize MFY[k] instead of Y[k].

[0036]   The combined FIR (i.e., the FIR filter being updated) includes coefficients
5   generated by the convolution of the main equalizing FIR, the matched filter and the error filter:

$$MFY = X * FIR\text{-filter} * Matched\text{-Filter} * Error\text{-Filter} \tag{7}$$

[0037]   In the present invention, the coefficients in the main FIR filter are to be adapted (see, e.g., step 122 in FIG. 3). The matched filter and error filter coefficients need not be adapted, but instead, may only be convolved (e.g., with a data signal) once their values are
10   determined. Consequently, a new algorithm has been created that takes these factors into consideration.

[0038]   For LMS-based adaptive filters to work effectively, the filter input and output should be available (e.g., to enable effective reception and transmission of equalized data). In addition, to take advantage of existing LMS update/adaptation rules, one may create or generate a
15   matched-filtered version of the unequalized data sequence X. To accomplish this, equation (7) above may be rearranged in the following way:

$$MFY = (X * Matched\text{-Filter} * Error\text{-Filter}) * FIR\text{-filter} \tag{8}$$

$$= MFX * FIR\text{-filter} \tag{9}$$

[0039]   In equations (8) and (9), MFY now becomes a vector available for adaptive LMS-
20   based filtering. The value of MFX = (X * Matched-Filter * Error-Filter) is not necessarily an available vector for adaptive filtering under these conditions, nor is it required to be, so it may be (and generally is) explicitly and separately computed. For example, and as shown in step 110 of

FIG. 3, the received digital data stream may be convolved with the matched filter and the error filter to generate a matched-filtered (but unequalized) data sequence MFX[k]. As is known in the art, the filter operations are commutative; i.e., the data stream may be convolved with the filters in any order.

5   **[0040]**   The algorithm may now be transformed into a form typical of a regular or conventional adaptive FIR filter, thereby enabling one to update the weighting coefficients in a LMS-based FIR filter algorithm. The adaptation recursion equation may thus become:

$$C0 = C0 + \mu * MFE[k] * MFX[k] \tag{10}$$

$$C1 = C1 + \mu * MFE[k] * MFX[k-1] \tag{11}$$

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$$\ldots$$

$$Cn = Cn + \mu * MFE[k] * MFX[k-n] \tag{12}$$

where MFE is the difference between MFY and its ideal noiseless value, MFYH. One may thus appreciate that an important aspect of the invention involves using structurally and/or functionally similar or identical filters to generate both the data term and the error term for the

15   adaptive FIR algorithm.

[0041]   MFE can be determined and/or generated by taking the difference between MFY and MFYH, preferably after correcting for the difference in the pipeline latencies of the various data receiving and/or processing blocks. FIG. 3 shows an exemplary sequence of process steps 114 and 116 for generating, determining and/or calculating MFYH. For example, equalized data

20   sequence Y may be processed by a conventional sequence detector (see, e.g., step 114), then convolved with a conventional target filter, a matched filter (preferably, identical in structure and function to the matched filters for the equalized data sequence Y in step 106 and the received

data sequence X in step 110), and an error filter (see, e.g., step 116; also preferably identical in structure and function to the error filter in steps 106 and 110).

[0042]   FIG. 3 shows the process for generating MFE in step 130.   Matched-filtered equalized data sequence MFY is subtracted from its ideal value MFYH using a conventional subtractor configured to operate on a data sequence having the length(s) of MFY and/or MFYH. Alternatively, MFY may be compared with MFYH in a conventional digital or analog comparator, and a value for any error in the equalized data signal may be determined using conventional digital and/or analog logic configured to do so. The error value can be incorporated into the adaptive FIR algorithm. For example, a comparison on digital signals may simply determine whether the equalized data and its corresponding ideal, noiseless value are the same or different, and if different, whether the difference is positive (e.g., 1) or negative (e.g., -1). A comparison of analog signals (or an analog comparison of digital signals) may involve comparing the equalized data and/or its corresponding ideal, noiseless value to each other or to a reference value, then amplifying the output of the comparison to obtain error data that can be used to update the FIR algorithm. Referring back to FIG. 3, the obtained MFE value is then used to update the FIR filter (along with the MFX[k] sequence) in step 122.

[0043]   Alternatively, a mathematically equivalent process for generating MFE involves subtracting YH from Y (similar to the process described in FIG. 2) to generate an error term, then convolving the error term with a single matched filter and a single error filter to generate MFE. This alternative process eliminates one filter block from the architecture (compare, e.g., FIGS. 6 and 8), and may reduce the number hardware changes to previous designs.

[0044]   Once the adaptive filtering algorithm has been converted into a form similar to the regular LMS gradient algorithm, the same techniques of simplification available for LMS can be applied to single bit error-optimized adaptive filtering. This includes using quantized values of MFX and/or MFE in place of their actual values. Thus, the (filtered) error and/or data terms for

the adaptive algorithm also include quantized versions of the (filtered) error term and/or the (filtered) data term. In addition, μ need not be continuously updated. Rather, updates and/or changes to μ can be qualified (or preconditioned) on predetermined states of data from the sequence detector (or other data processing block configured to determine an actual value of data

5   in the data sequence), or on changes in such data.

[0045]   Referring now to FIG. 4A, an example of single bit error detection is shown. Received data stream S (corresponding to received data signal X above) has the particular value shown (e.g., 0,0,0,1,0,0,0,0). While the length of received data stream S is shown to be 8 bits, or 1 byte, this length can be any length conventionally used in the given application and/or for

10   which appropriate data signal processing technology exists. Of course, the bits in received data stream S may have any conventional digital or analog value.

[0046]   However, processing by signal processing circuitry (e.g., a conventional sequence detector and target filter) may determine that the ideal, noiseless value for S should be a value in which one bit differs. The ideal, noiseless value for S is shown in FIG. 3 as S_exp, or its

15   expected value (e.g., 0,0,0,0,0,0,0,0). The error value *error* (e.g., 0,0,0,1,0,0,0,0) is determined by subtracting S_exp from S, and the FIR filter is modified to reflect a new C(4) value in accordance with conventional techniques (see, e.g., "Digital Baseband Transmission and Recording," by J.W.M. Bergmans, Kluwer Academic Publishers, Dordrecht, The Netherlands (1996), pp. 373-450, the relevant portions of which are incorporated herein by reference).

20   [0047]   FIG. 4B shows a complementary error (i.e., one in which the error value *error* is 0,0,0,-1,0,0,0,0). While the actual value of *error* in FIG. 4B differs from that in FIG. 4A, its absolute value is the same. Consequently, the same result (i.e., updating the FIR algorithm coefficient) will be obtained. Thus, the single bit error function employed in this embodiment of the present filtering method and algorithm effectively minimizes single bit error events.

[0048]   Referring now to FIG. 5, two examples of dibit error detection are shown. Received data stream S has the particular value shown (e.g., 0,1 or 1,0). In contrast, S_exp (e.g., the ideal, noiseless value of S) is determined to be (1,0) or (0,1), respectively. The error value *error* is thus (-1,1) or (1,-1), respectively.

5   [0049]   While the concept of the invention is to target the adaptive algorithm to minimize predominant error events, the exemplary embodiment of the invention described herein is ideally suited to minimizing single bit error events. For those error events that may not be targeted and/or optimally minimized in the present method and/or algorithm, a second and/or different adaptation algorithm can be employed to thereby minimize infrequent, secondary or less

10   significant RMS errors.

Exemplary Software

[0050]   Although the description herein tends to focus on methods and hardware (e.g., architectures, systems and/or circuits), the present invention also includes a computer program and/or software, implementable and/or executable in a general purpose computer or workstation

15   equipped with a conventional digital signal processor, configured to perform one or more steps of the method and/or one or more operations of the hardware. Thus, a further aspect of the invention relates to software that implements the above method and/or algorithm. For example, the invention may further relate to a computer program, computer-readable medium or waveform containing a set of instructions which, when executed by an appropriate signal processing device,

20   is configured to perform the above-described method and/or algorithm.

[0051]   For example, the computer-readable medium may comprise any medium that can be read by a signal processing device configured to read the medium and execute code stored thereon or therein, such as a floppy disk, CD-ROM, magnetic tape or hard disk drive. Such code may comprise object code, source code and/or binary code.

[0052]   The waveform is generally configured for transmission through an appropriate medium, such as copper wire, a conventional network cable, a conventional optical data transmission cable, or even air or a vacuum (e.g., outer space) for wireless signal transmissions. The waveform and/or code are generally digital, and are generally configured for processing by a

5   conventional digital data processor (e.g., a microprocessor, microcontroller, or logic circuit such as a programmable gate array, programmable logic circuit/device or application-specific [integrated] circuit).

Exemplary Architectures

[0053]   The present signal processing architecture generally comprises (i) an equalizer

10   configured to equalize and/or filter a data sequence in accordance with an adaptive algorithm and provide an equalized data output; (ii) a first filter, configured to receive the data sequence and generate a filtered data term for the adaptive algorithm; and (iii) an error term circuit, configured to receive the equalized data output and provide a filtered error term for the adaptive algorithm, the error term circuit comprising a second filter having filter characteristics similar to the first

15   filter. Thus, the present architecture may be implemented as circuitry or circuit blocks on one or more integrated circuits, as a hardware description of a circuit (e.g., in VHDL or a Verilog® description), in a monolithic integrated circuit, or in a plurality of discrete devices on a circuit board.

[0054]   FIG. 6 shows a first exemplary architecture 150, configured to implement and/or

20   execute the above method, algorithm and/or software. This embodiment includes FIR filter 152, matched filter blocks 154a, 154b and 154c, error filter blocks 156a, 156b and 156c, sequence detector 158 and target filter 160.

[0055]   In essence, architecture 150 comprises three signal processing paths: (1) a first filtering path configured to generate a matched-filtered data signal MFX from received data X,

25   (2) a second filtering path configured to generate a matched-filtered equalized data signal MFY

from equalized data Y, and (3) an equalized data processing path configured to generate an ideal, noiseless equalized data signal MFYH from equalized data Y. Each such path comprises a filter block including a matched filter 154 and an error filter 156. In one implementation, each of matched filter blocks 154a, 154b and 154c are structurally and/or functionally identical to each

5   other. In a further implementation, each of error filter blocks 156a, 156b and 156c are structurally and/or functionally identical to each other. In a preferred embodiment, the architecture further includes a conventional adaptive FIR filter 152. More specifically, the second filtering path further includes adaptive FIR filter 152, and is configured to generate a matched-filtered equalized data signal MFY from received data X.

10 **[0056]**   FIG. 7 shows an embodiment of a circuit and/or architecture 170 that updates the LMS algorithm of the adaptive FIR filter 152 using matched-filtered equalized data signal MFY and ideal, noiseless equalized data signal MFYH. For example, a subtractor 175 may be configured to receive the two signals MFY and MFYH. As described above, subtractor 175 may subtract ideal, noiseless signal MFYH from signal MFY. Alternatively, and particularly when

15 the signals are digital, signal MFY may be subtracted from ideal, noiseless signal MFYH, but the former configuration is preferred over the latter. Also, a conventional comparator configured to operate on the two signals MFY and MFYH as described above with regard to the present method may be substituted for subtractor 175.

[0057]   As described above, the difference between MFY and MFYH may comprise

20 MFE[k], the matched-filtered error term used to update the adaptive algorithm employed in FIR filter 152. When MFY and MFYH are the same, MFE is zero, and coefficient adaptation block 180 does not change the adaptive FIR algorithm. When MFY and MFYH are not identical, MFE is non-zero, and coefficient adaptation block 180 may modify or change the adaptive algorithm. However, even when MFE is zero, coefficient adaptation block 180 may be continuously or

25 periodically updating the adaptive FIR algorithm.

[0058]   In another aspect, the present invention concerns an alternative architecture configured to implement adaptive FIR filtering that includes a FIR filter, a data signal processor, a matched filter block, and a conventional subtractor circuit. An example of such an architecture is shown in FIG. 8.

5   [0059]   As for the first architecture embodiment, in the architecture 200 of FIG. 8, a data signal X is received by a conventional data signal receiving apparatus, device, circuit or circuit block (not shown), and input into one or more functional blocks. One such functional block is FIR filter 202, configured to output an equalized data signal D_{OUT}. The equalized data signal D_{OUT} may also be input into subtractor block 208.

10   [0060]   Alternatively or additionally, equalized data signal D_{OUT} may be input into a signal processing block 230. In a preferred embodiment, signal processing block 230 comprises a conventional sequence detector 210 and a conventional target filter 212, although any processor block configured to perform a data signal processing operation on a received data signal may be employed. More specifically, and in accordance with the above method and algorithm, sequence

15   detector 210 is configured to receive equalized data signal D_{OUT}, and conventional target filter 212 is configured to be convolved with equalized data signal D_{OUT} after sequence detection. Alternatively, target filter 212 may be configured to receive equalized data signal D_{OUT}, and conventional sequence detector 210 may be convolved with equalized data signal D_{OUT} after target filtering. The output of signal processing block 230 may be input into subtractor block 208

20   for comparison to and/or subtraction from equalized data signal D_{OUT}. Architecture 200 may further comprise a conventional channel selector block 214, configured to select a target channel in the receiver and provide corresponding filter function and/or algorithm information to target filter block 212.

[0061]   Matched filter block 220a may comprise matched filter 204a and error filter 206a.

25   Matched filter 204a receives the output from subtractor block 208, and error filter 206a may be

configured to receive the output from matched filter 204a. Alternatively, error filter 206a may be configured to receive the output from subtractor block 208, and matched filter 204a may be configured to receive the output from error filter 206a. In either case, the output of matched filter block 220a is the error term for the adaptive FIR algorithm, MFE[k].

5   [0062]   Alternatively, subtractor 208 may be replaced with a conventional digital or analog comparator, optionally including logic sufficient to determine a value for any error in the equalized data signal, where the error value can be incorporated into the adaptive FIR algorithm after convolution with matched filter block 220a. The conventional digital comparator may simply comprise digital logic gates configured to determine whether the equalized data and its

10   corresponding ideal, noiseless value are the same or different, and if different, whether the difference is positive (e.g., 1) or negative (e.g., -1).

[0063]   Received data signal X is also processed by a matched filter block 220b, which is similar (and preferably, identical) in structure and function to matched filter block 220a. Thus, one key to the invention is processing of the error term and of the data signal by functionally

15   and/or structurally similar or identical filters. As one can easily see, the common structures to the various data signal processing paths in the exemplary architectures of FIGS. 6 and 7 are the matched filter and error filter.

[0064]   Of course, the architecture may further comprise any of the function blocks disclosed herein. For example, the architecture may further comprise a FIR filter, a signal

20   processor (which, in turn, may comprise a sequence detector and/or a target filter), and/or a subtractor or comparator. The filter circuitry is generally conventional, and typically includes a conventional adder and/or multiplier, depending on the function(s) and/or mathematical operation(s) to be performed.

An Exemplary System and Network

[0065]   A further aspect of the present invention concerns systems for reading magnetically recorded data, generally including the architecture and, for example, a receiver and/or magnetic recording device. In one embodiment, the system comprises the present signal processing architecture and at least one receiver communicatively coupled to the architecture for receiving a data signal.

[0066]   The present system may further include details of the architectures described above. For example, the system may include an equalizer that comprises an adaptive finite impulse response (FIR) filter. Preferably, the adaptive FIR filter employs a least-mean-square (LMS) algorithm. The system may also include a signal processor that comprises a sequence detector and/or a target filter; an error filter configured to receive the matched filtered output and/or to minimize single bit error events, a dibit error event, and/or a tribit error event.

[0067]   The system may further comprise a second matched filter, configured to receive signal-processed (e.g., sequence detected) data and provide matched-filtered processed data. Preferably, the system further comprises a third matched filter, configured to receive the incoming data stream and provide a matched-filtered (received) data signal. In such embodiments, the system preferably also comprises (1) a second error filter configured to receive the matched filtered processed data and output an ideal matched filtered output, and/or (2) a third error filter configured to receive the matched filtered data signal and provide an equalizer algorithm component.

[0068]   The system may also further comprise a subtractor configured to receive the matched-filtered output and the ideal matched filtered output. While the subtractor generally subtracts one of the matched-filtered output and the ideal matched filtered output from the other,

it preferably subtracts the ideal matched filtered output from the matched-filtered output. The subtractor may provide the update signal that updates or modifies the LMS algorithm in the FIR filter. Alternatively, the subtractor may be replaced by a comparator configured to compare the matched-filtered output and the ideal matched filtered output, but the subtractor implementation

5   is preferred.

[0069]   The invention also relates to a magnetic recording system, comprising the present system and a magnetic storage device, communicatively coupled to the system. The magnetic storage device may comprise a floppy disk, a CD-ROM, a magnetic tape or a hard disk drive. The system may be part of a read channel device. The present magnetic recording system and/or

10   device may employ the matched-filtered LMS algorithm and filtering method described in detail above.

CONCLUSION / SUMMARY

[0070]   Thus, the present invention provides a method, algorithm, software, architecture, system and circuit for adaptively filtering a received data signal that targets certain predominant

15   error events for minimization. The error events to be minimized are generally those that occur most often in a given data signal processing application. For example, single bit error events in sequence detection occur most frequently in reading magnetically recorded data. Thus, an adaptive algorithm targeting single bit error events for minimization in magnetic media read applications will converge much more rapidly than a conventional LMS algorithm without

20   significantly sacrificing quality (particularly if one or more additional algorithms are used to target the secondary error events).

[0071]   The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many

modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is

5   intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.